摘要

AVS 的应用推广伴随着技术的日趋成熟已经走过了十年，在新形势下，高性能的 AVS 高清编码芯片的开发成为其进一步开拓市场的关键。本文就是从实际多媒体芯片的设计出发，研究了 AVS 编码芯片设计中与帧内技术相关的编码重要环节，包括帧内预测，帧内模式决策，编码等几个部分。探索在硬件设计速度、面积、性能等多维约束的情况下帧内编码的实现方法，对结构做了优化设计，使与帧内编码相关的算法以芯片设计的手段实现。本文的创新点如下：

首先，针对 AVS-P2 中帧内预测的算法，设计了一套高速的并行预测结构。该结构支持包括亮度块和色度块在内帧内预测垂直、水平、DC、左下对角、右下对角、平面六种模式的预测，可以高速地并行输出一个块的所有模式预测数据，另外，本结构具有很强的复用性，可以使用不同的参考像素进行预测。

其次，针对帧内模式决策做了重点分析与设计，用系统模型对主要的帧内模式决策方法进行了性能上的分析，然后针对块级数据编码流水线，同时也是 RDO 决策的块级数据流水线进行了深入细致的分析。根据其特定的功能模块的时间开销，设计了八路并行的块级流水结构，从理论上阐述了五级流水编码流水线的合理性，并给出了一种基于RDO帧内模式决策高效的流水调度方法，突破了在RDO条件下，由于帧内预测对重构数据的依赖而打断流水线的技术障碍。另外，也给出了基于 SAD 的帧内模式决策结构与方法。

再次，为完成对于整个帧内编码的设计，结合本文所提出的高效哥伦布编码单元和宏块头编码单元，设计了对最后的编码环节宏块码流生成部分进行了结构设计，实现了实时流水编码。

最后，综合以上三方面的研究成果，灵活运用之前所设计的帧内编码关键单元，从速度优先的角度设计了基于 SAD 的帧内编码系统，以及从编码质量优先的角度设计了基于 RDO 的帧内编码系统，并比较了两者的优劣。

关键词：AVS，编码芯片结构，帧内预测，帧内模式决策，码流生成，流水线

The architecture design and algorithm implementation of intra prediction and encoding for AVS

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Abstract

AVS applications and market promotion has gone through ten years along with the technology maturing day and day. The development of high performance AVS HD encoder chip has become the key to further develop the market in the new situation. This article is from the actual multimedia chip design. Several important modules about intra technology are researched, including intra prediction, intra mode decidion and bits stream generator etc. A optimized intra encoding architecture is designed, so that the intra encoding algorithm is put into practice with multi-dimensional constraints such as speed, area and encoding quality etc.. The innovation of this paper is as follows:

Firstly, A high-speed parallel intra prediction structure is designed based on the algorithm for AVS-P2, the structure supports all intra mode of luminance and chrominance blocks, including vertical mode, horizontal mode, DC mode, down left mode, down right mode and plane mode. It can output all prediction data of all modes that belong to one block at the same time. Moreover, the structure has a strong reusability, different reference pixels can be used to predict.

Secondly, focusing on analysis and design for intra mode decision. First of all, performance analysis of the main intra mode decision method is carried out with the help of the system C model. Then the deep and detailed analysis is given for block-level data encoding pipeline, but also the pipeline of the mode decision based on RDO. Eight parallel block-level pipeline structure is designed according to the time cost of specific functional modules. Further more, the article theoretically expounded the rationality of the five states encoding pipeline, and gives an efficient scheduling method of intra mode decision pipeline based on RDO, breaking the technical barriers that the pipeline of RDO is interrupted, due to the intra prediction on the dependence of the

reconstruction data. In addition, structures and methods based on the SAD are designed for intra mode decision.

Thirdly, in order to complete the design for the entire intra encoding, combined with the efficient the Columbus coding unit and the macro block header encoding unit, the architecture of the macro block bits stream generator, the last part of the intra encoder, is designed, realizing real-time encoding.

Finally, to sum up the above three aspects of research, and flexible using the important proposed units of intra encoder, Intra encoding system based on the SAD is designed from the point of the speed priority, as well as the system based on the RDO is proposed from the other point of the quality priority. The pros and cons of both are analyzed and compared.

Keywords: AVS, encoding chip architecture, intra prediction, intra mode decision, bits stream generator, pipeline.